NEUVIEME COLLOQUE SUR LE TRAITEMENT DU
SIGNAL ET SES APPLICATIONS

NICE du 16 au 20 MAI 1983

PERFORMANCE IMPROVEMENT OF A BINARY QUANTIZED ALL-DIGITAL PHASE-LOCKED LOOP WITH A NEW AIDED-ACQUISITION TECHNIQUE

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RESUME

A non-uniform sampling digital phase-locked loop (DPLL) is proposed with a sequential loop filter, in which two additional phase comparators are added conjointly with an estimation-decision circuit to provide more freedom to deal with the conflicting requirements of minimum acquisition time and maximum noise rejection.

Using a pseudo-two-dimensional random-walk-filter, the stationary phase error variance and the mean acquisition time have been evaluated. The comparison between the theoretical analysis and the experiments has proven to be very satisfactory. Substantial reduction of the acquisition time, without severely degrading the noise reduction performance has been achieved.

A digital loop "quasi-bandwidth" measure was used in the evaluation of the loop performance, thus allowing for a comparison with other digital loops and to a limited extent with a first order analog loop. The usual difference in performance favoring the analog loop for high signal-to-noise ratio is shown to be substantially reduced and can be lowered by an appropriate choice of parameters. The hardware needed for the implementation of the modified DPLL is shown to be very simple.

SUMMARY

Un échantillonneur non-uniforme avec verrouillage de phase numérique est proposé. Il comporte une boucle de filtrage séquentielle dans laquelle deux comparateurs de phase ont été introduits de même qu'un circuit "estimation-décision". Cet arrangement permet plus de liberté lorsqu'on est en présence du choix entre les exigences du temps minimum d'acquisition et l'élimination maximum du bruit.

En utilisant un compteur-décompteur à marche aléatoire, la variance de l'erreur stationnaire de phase et la moyenne du temps d'acquisition ont été évaluées.

La comparaison entre l'analyse théorique et les simulations numériques donne d'excellents résultats. Une réduction appréciable du temps d'acquisition a pu être obtenue sans détérioration des performances du système en ce qui concerne le bruit.

Une mesure de boucle numérique "quasi-passe-bande" a été utilisée pour l'évaluation du dispositif. De ce fait une comparaison avec d'autres systèmes de boucle à verrouillage de phase aussi bien numériques qu'analogiques a été effectuée. La différence de qualité favorable au système analogique en ce qui concerne le rapport signal-sur-bruit, peut être diminuée substantiellement en choisissant les paramètres d'une façon adéquate.

Le circuit requis pour la réalisation de ce système se trouve être relativement simple.

INTRODUCTION

Phase-locked loops play an important role in transmission systems, more particularly for the recovery of the carrier phase and symbol timing in synchronous detection, in order to reduce the probability of error of the received symbols to a minimum. With the development of "Large Scale Integration" in digital communication systems and subsystems, the DPLL's are rapidly replacing their analog counter parts. A recent survey of DPLL's [1] has demonstrated that even with a rather large variety of implementation, the performance can still be improved upon. With DPLL systems, the designer is usually faced with different requirements such as minimum phase error variance, small acquisition time and maximum locking-range and he must also produce an inexpensive, flexible and reliable design. Some solutions to these basic but yet conflicting requirements are reported by Yamamoto and Mori [2] and Andrea and Russo [3]. Recently, Heiman and Bar-Ness [4] have demonstrated "that by adding another phase detector, the system can be provided with enough additional freedom to be able to better deal with these conflicting requirements and yield smaller errors".

The purpose of this paper is to improve the tracking and acquisition behavior of the improved DPLL proposed by Andrea and Russo [3] by adding a third phase comparator and a random-walk-filter [5]. The additions will allow this modified DPLL (3PDPLL) to decide whether it is either in acquisition or tracking mode resulting in large or small phase steps, respectively, in the process of phase correction.

The main feature of the graphical analysis in the absence of noise is to give some physical insight into the acquisition and tracking behavior. With the noise taken into account, a mathematical model is derived following [2], [5] and the random-walk technique of [5],[6], [7] is applied to evaluate the RMS phase error and the mean acquisition time. Experimental results confirm the appropriate simplifying hypothesis used in the numerical analysis.

A performance criterion defined in terms of the RMS phase error and the acquisition time (which is closely related to the bandwidth of the loop) for a given signal-to-noise ratio is used. It provides a common basis for comparison of different digital loops and, to a limited extent, also with a first order linear loop.

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Proposed Digital Phase Locked Loop

The proposed DPLL is shown in Fig. 1. The overall input signal x(t) is defined as:

$$x(t) = s(t) + n(t) \qquad (1)$$

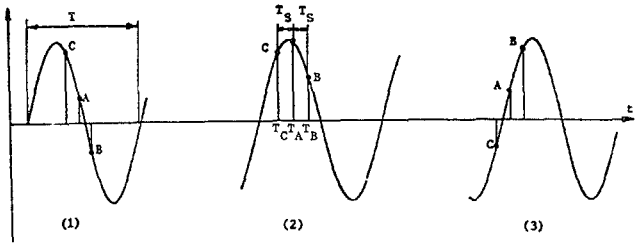
where s(t) and n(t) are the signal and the noise terms respectively. The samples are taken in sets of three every k (integer number)cycles of the signal s(t).

The DPLL itself can be described as a First-Order Transition Sampling DPLL using a Random Walk Filter with the addition of an estimation-decision circuit controlling the state in which the loop is to work. We define two possible states as follows:

(1) Acquisition, resulting in the use of larger step corrections (wider bandwidth)

(2) Tracking, resulting in the use of smaller step corrections (narrower bandwidth)

Graphical Analysis in the Absence of Noise



T_A: Sample time of A

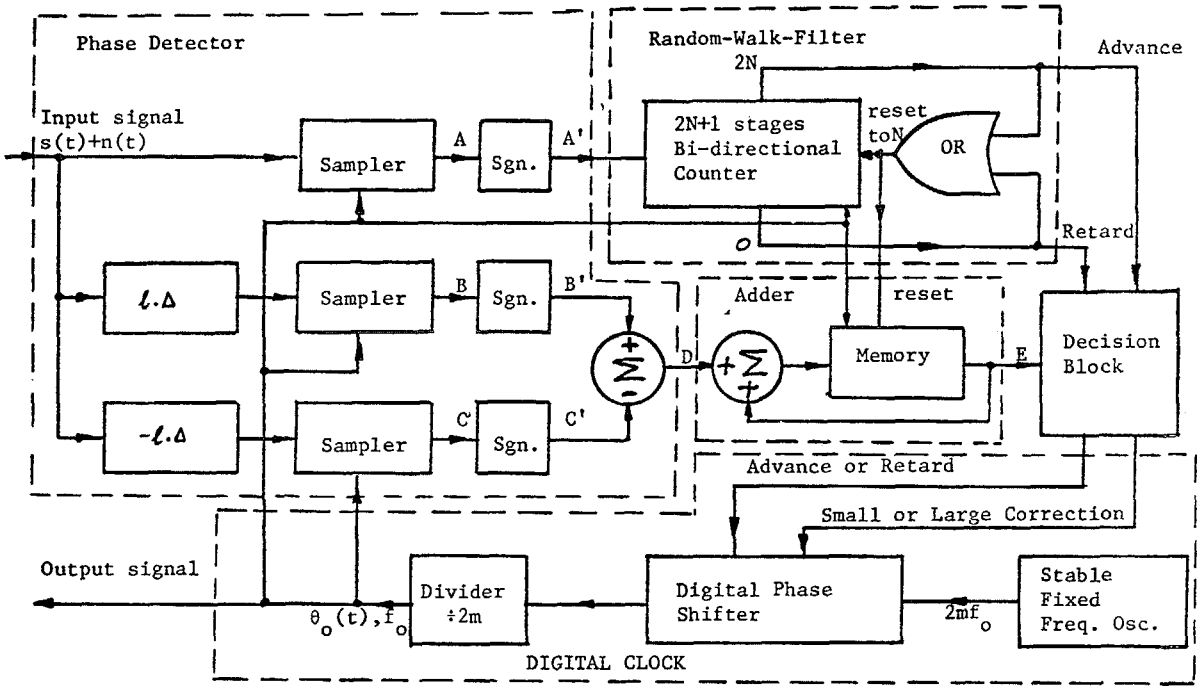
T_B: Sample time of B

T_C: Sample time of C

T_S: Time between 2 samples in a same set

$T_S = T\ell\Delta/2\Pi$

Fig. 2 - Examples of three different cases of samples [A, B, C]



Where

- 2m: number of phase states per cycle
- $\Delta=\Pi/m$: size of the unit phase step
- ℓ: integer number of unit phase steps (defines the distance between the three samples)
- n: ratio between the large ($n\Delta$) and the small (Δ) corrections (integer number)
- 2N+1: random-walk filter length
- $\theta_o(t)$: output phase
- $\theta_i(t)$: phase of s(t)
- $\Phi(t)$: phase error ($\theta_i(t)-\theta_o(t)$)

Fig. 1 - Block Diagram of the 3 PDPLL

	(1)	(2)	(3)	(4)	(5)	(6)
A'	+1	+1	+1	-1	-1	-1
B'	-1	+1	+1	+1	-1	-1
C'	+1	+1	-1	-1	-1	+1
D	-2	0	+2	+2	0	-2

A' = Sgn A, B' = Sgn B, C' = Sgn C, D = B'-C'

Table 1 - Values of D in function of the samples [A, B, C]

The information at point D (Fig. 1) appearing as a difference of the signed values and shifted input signal x(t) increments or decrements an adder. Its output (E) is used when the random walk filter gives a command of advance or retard as a criterion for the size of the correction.

From Fig. 2 and Table 1, we observe that there are only six possible outcomes for A'B'C' and only three corresponding outcomes for D (-2, 0, +2). If the PLL is assumed to track the positive zero crossings of x(t) then we can define the two possible states as a function of D which can be translated into an appropriate

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choice of correction size (i.e. loop gain) as follows:

State	Value of D	Correction size
Acquisition	-2, 0	$n\Delta = n \cdot 180°/m$
Tracking	+2	$\Delta = 180°/m$

where n(an integer) is the ratio of the two correction sizes.

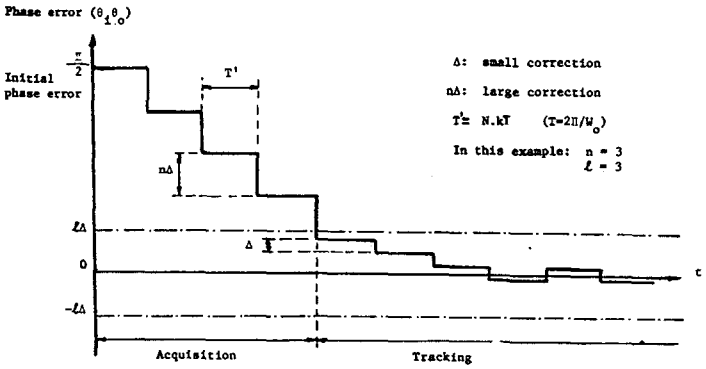

Fig. 3 - Example of "Acquisition" and "Tracking" (noise free case)

In Fig. 3, the mechanism of synchronization is depicted for an initial phase error of approximately 90°. As illustrated, once the acquisition is completed, the correction size is reduced and the tracking takes over. The maximum phase error is equal to the minimum size Δ of the correction (Δ = 180°/m).

Mathematical Model in the Presence of Noise

The signal and the noise terms of equation (1) can be written as

$$s(t) = A \sin [\omega_o t + \theta_i(t)] \qquad (2)$$

$$n(t) = n_s(t) \sin \omega_o t + n_c(t) \cos \omega_o t \qquad (3)$$

The input signal s(t) is supposed to be sinusoidal of known angular frequency ω_o and of unknown phase $\theta_i(t)$ (which is to be recovered by the PLL) perturbed by random noise n(t) representing a narrowband Gaussian noise process of zero mean and of variance σ^2. We assume that the bandwidth is sufficiently large so that the samples of n(t) can be regarded as independent between k (integer number) cycles of s(t) but narrow enough such that within a small interval $2\Delta t$ in a cycle of s(t) both $n_s(t)$ and $n_c(t)$ will approximately be constant. These assumptions can be stated as follows:

$$n_s(t_1) \simeq n_s(t_1+T_s) \simeq n_s(t_1-T_s)$$

$$n_s(t_1+kT) \simeq n_s(t_1+kT+T_s) \simeq n_s(t+kT-T_s) \qquad (4)$$

and

$$n_s(t_1) = n_s(t_1+kT) \qquad \text{(no correlation)} \qquad (5)$$

(similar equations can be defined for $n_c(t)$)

It can be shown that for each set of samples, A, B and C (Fig. 1) are statistically dependent and the joint probabilities of occurrences of A', B' and C' can be computed for all possible phase errors by using the probability density of the phase for a sine wave plus Gaussian noise [8].

Following the procedure of Cessna and Levy [5], the 2n possible phase error conditions can be modelled with a Markov chain.

The derived general state transition model for the DPLL (Fig. 4) is used to compute the RMS phase error and the mean acquisition time. Fig. 5 represents the state transition model for one particular phase error (stage). There are 2 m such stages.

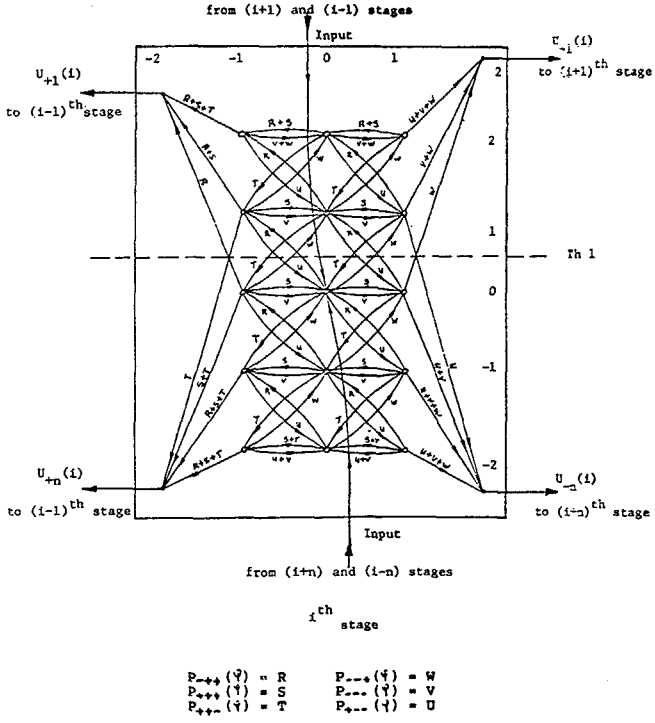

Fig. 5 - Example of the state transition model of one stage (N=2, Th=1)

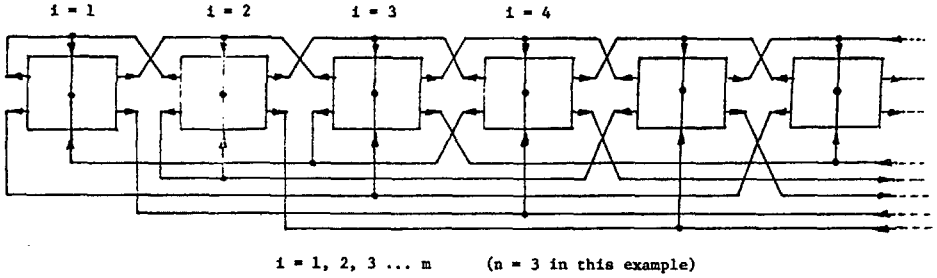

Fig. 4 - General state transition model composed of m stages

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Due to the complexity of the model, the termination probabilities $U_{-1}(i)$, $U_{-n}(i)$, $U_{+1}(i)$ and $U_{+n}(i)$ are numerically obtained by starting at the input with probability 1 and letting the propagation continue until nearly nothing is left in the model. The outputs accumulated at the four exit points will approximate the termination probabilities. The dimension of this array and the position of the threshold are parameters that can be chosen within the limits imposed by hardware considerations so as to obtain the desired performance.

The state selection probabilities and the average time spent in each stage are numerically computed and used to obtain the absolute state probabilities and the RMS phase error.

The mean acquisition time T_m is defined as the average time taken by the binary digital loop to reach the minimum possible value of phase error assuming equally likely probabilities of initial phase errors. The acquisition time $T_o(i)$ is defined as Tm but with the initial phase error Φ_i given. It is shown [5] that the T_o (i)'s can be obtained by solving a set of difference equations and that T_m is the average over all possible acquisition time $T_o(i)$.

Numerical and Experimental Results

Digital computer programs have been developed to obtain the RMS phase-error and the mean acquisition time for various examples of sequential filters and decision criteria. Selected examples and their performance are depicted in Fig. 6 and 7. The SNR at the input of the DPLL is defined as:

$$SNR = A^2 / 2\sigma_n^2 \qquad (6)$$

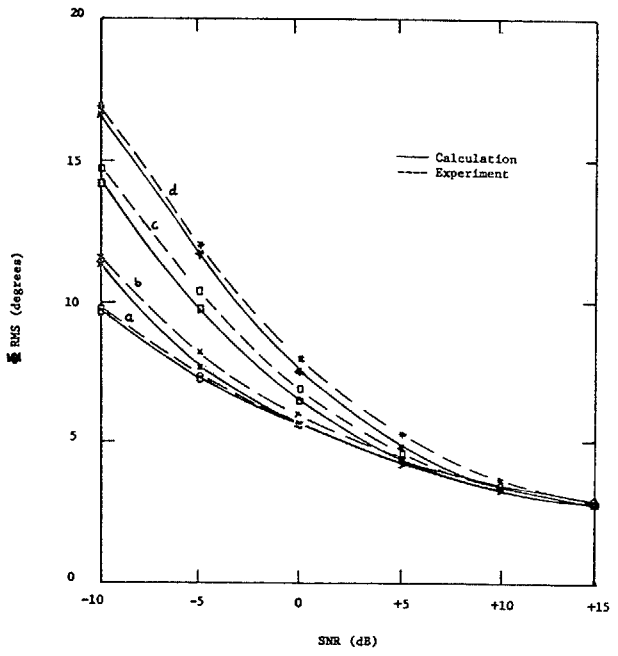

Fig. 6 - Loop RMS phase error versus SNR

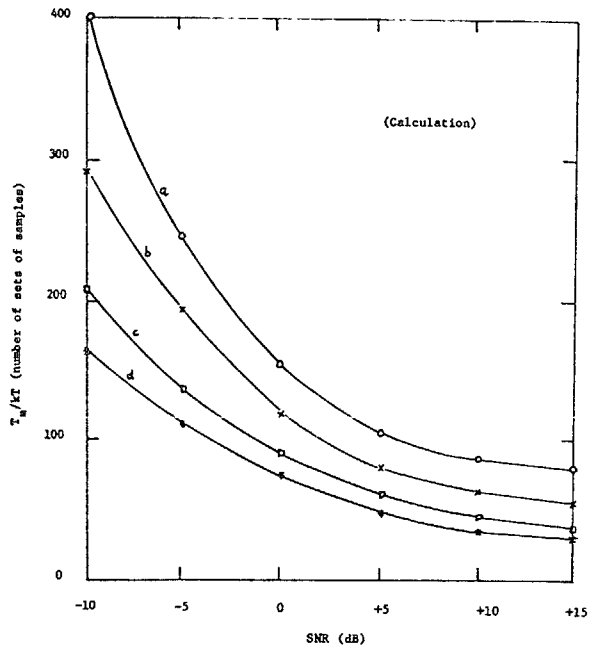

Fig. 7 - Mean acquisition time versus SNR

The four cases represented have the following parameters:

	N	Threshold	m	ℓ	n (ratio of the correction sizes)
a	5	-	32	-	1
b	6	Th2	32	2	2
c	6	Th2	32	2	3
d	6	Th2	32	2	4

The corresponding overall locking-range B_o, the mean acquisition time T_m and the RMS phase error Φ_{RMS} in noise free condition (k=1) are presented in the following table:

	B_o	T_m	Φ_{RMS}	
a	0.00625 f_o	80 T	3.25°	$\left(T = \frac{1}{f_o}\right)$
b	0.0104 f_o	48 T	3.25°	
c	0.0156 f_o	32 T	3.25°	
d	0.0208 f_o	24 T	3.25°	

where B_o and T_m are approximated as follows:

$$B_o \simeq f_o \frac{n}{mNk} \quad (7) \quad \text{and} \quad T_m \simeq kT \frac{N \cdot m}{2 \cdot n} \quad (8)$$

An experimental system based on a SDK 85 microprocessor has been set up to measure the RMS phase error and the results (Fig. 6) confirm the choice of symplifying hypothesis (4) and (5) used for numerical analysis.

A hardware realization of the 3PDPLL is shown in Fig. 8. It is worth noting that the block "Phase Detector" (Fig. 1) can be practically realized with a single hard-limiter if the two reversible counters composing both the random-walk-filter and the adder blocks are appropriately clocked.

As it can be seen, case a is equal to a convention-

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al DPLL with one phase detector and a sequential filter. Its performance can be compared against the new 3PDPLL. In cases a and b, the RMS phase error is approximately the same for a SNR of -5dB and up; but the corresponding acquisition times are decreased by about 20 to 30% for the 3 PDPLL. Cases c and d provide up to 60% improvement in acquisition time over the range of SNR's above +5dB for nearly equally good noise rejection performances. By varying the adjustable parameters, the user is provided with means of adapting the performance to some desired values (whether locally or over a wide range).

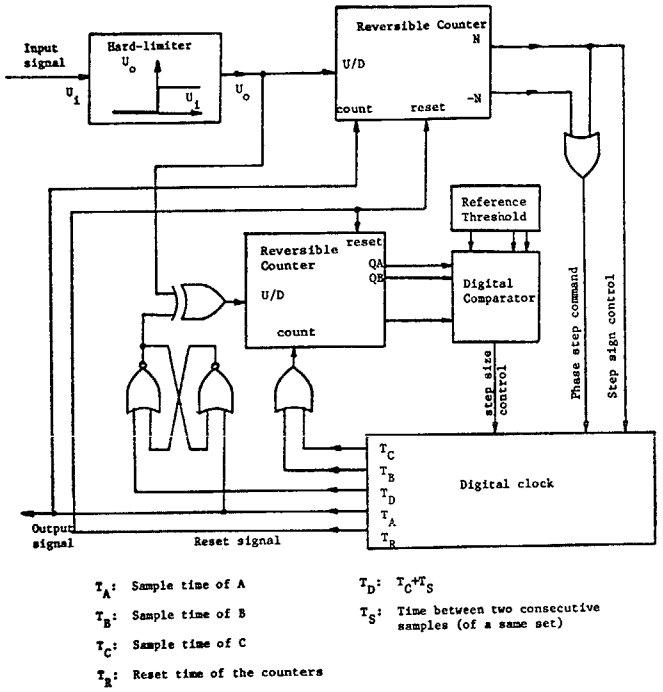

Fig. 8 - Hardware realization of the 3 PDPLL

Performance Comparison

In order to help the designer in his choice of DPLL systems, meaningful criteria need to be used to compare the digital loops and also with analog loops. One criteria has already been proposed by Cessna and Levy and will be briefly presented as in [5] as well as under a modified form. This criteria relates the RMS phase error to the signal-to-noise ratio in a given loop noise bandwidth B_L. For an analog PLL, the linear analysis [9] yields:

$$\Phi_{RMS} = \sqrt{\frac{N_o B_L}{P_s}} \quad \text{(rad)} \tag{9}$$

where

P_S : is the signal power
$N_o = \sigma_n^2/B_n$: is the one-sided noise power spectral density at the input of the PLL (10)
B_L : is the loop bandwidth

The DPLL being inherently non-linear, its loop bandwidth B' is a function of the SNR and thus cannot easily be defined from the loop parameters. The "Quasi-bandwidth" measure mentioned in [5] is based on the fact that B_L can be approximated by the inverse of the mean time for the loop to traverse a reference angular displacement of $\Pi/4$. That is:

$$B' = 1/kT\ T_o(m/4) \tag{11}$$

From (6), (9) and (11), a "Performance criterion" measure $Q(A^2/2\sigma_n^2)$ is defined:

$$Q(A^2/2\sigma_n^2) = \Phi_{RMS}(A^2/2\sigma_n^2)\sqrt{T_m(A^2/2\sigma_n^2)/kT} \tag{12}$$

The best performance is obtained for the smallest Q for a given SNR, when the designer tries to minimize both the RMS phase error and the mean acquisition time. The performance criterion for the conventional DPLL with one phase detector and a sequential filter and the 3PDPLL are compared with that of the linear analog model against signal-to-noise ratio in Fig. 9.

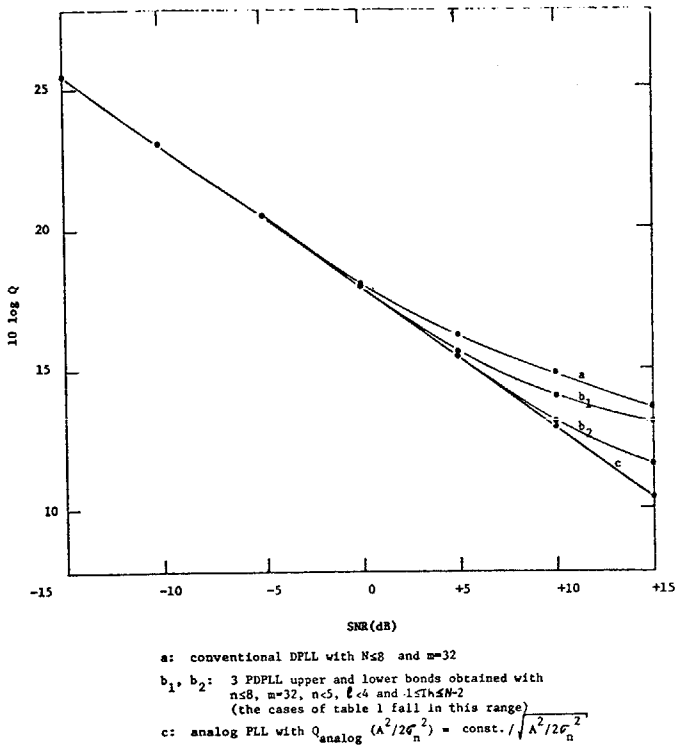

Fig. 9 - Performance criteria vs. SNR

It is significant to note that all the values obtained for the different combinations of parameters (n, Th, 1, N, m) fall within the bounds defined by b_1 and b_2. Moreover, for low signal-to-noise ratio (less than 0dB), all the curves have roughly the same slope while for high signal-to-noise ratio the difference in performances favoring the analog loops is shown to be substantially reduced for the 3PDPLL.

CONCLUSION

The non-uniform sampling DPLL with sequential loop filter in which the correction sizes are controlled by the accumulated differences of two additional phase comparators has been analysed. The numerical and experimental results have confirmed the expected reduction of the acquisition time and the small degradation of the noise rejection performances. Furthermore, the hardware needed to implement the 3PDPLL has been shown to be very simple.

A loop "Performance Criterion" was successfully used to compare DPLL's and illustrate the advantages and limitations of the 3PDPLL. Specifically the improvement of the performance which approaches that of an analog PLL for high signal-to-noise ratio.

These promising results leave the door open for further investigation. Applications in carrier phase and bit timing recovery are to be investigated as these will benefit from the improved performance parameters.

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Acknowledgement

Support from the Natural Sciences and Engineering Research Council under Grant A8572 and Strategic Grant G0665 is gratefully acknowledged.