IMPLEMENTATION OF 2400 bps VOICEBAND DATA MODEM USING THE DSP TS68930

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Dans cet article nous décrivons les différentes étapes suivies depuis la simulation jusqu'à l'implémentation d'un modem à 2400 bits par seconde, en l'occurence le V22 bis.
L'implémentation est faite sur le processeur de signaux TS68930 de S.G.S-Thomson.Ce processeur présente les particularités suivantes: architecture harvard, flot de données en pipeline,fonctionnement en parallèle des unités de calculs, possibilité de calcul en mode complexe. La première étape a consisté en une simulation globale de toutes les fonctions du modem en langage évolué. Elle a permis par son intéractivité l'optimisation des différents paramétres. Nous avons en outre procédé à une simulation pour évaluer les effets d'arrondi et de troncature avant l'implémentation sur le composant.

The present paper describes the different steps followed from the simulation to the integration of a medium speed V22bis voiceband data modem on the S.G.S-Thomson TS 68930 digital signal processor (DSP). The choice motivations for this DSP are mainly the computational performance and facilities it offers. It features a 3-bus structure, pipeline data flow, Harvard memory spaces, parallel processing and the possibility of complex computations. The first step before the implementation on the DSP, was to perform a global simulation in a high level language which permits to optimise the different parameters. To analyse the effect of finite word lenght and variable dynamics, simulation has been carried out. It performs in the Fortran language all processor computations, troncatures and normalisations. It is shown that high performance was obtained with only one single DSP without any external hardware.

1. INTRODUCTION

With the recent advances in semiconductor technology, several possibilities are given to implement digital modems on a single chip . The custom VLSI realizations offer the most economical way for its realization as far as large series are concerned.

The main aim of this work is to develop an efficient and software-oriented solution which makes possible the implementation of several transmitters and several receivers on the same DSP. While the heart of the modem lies in its signal-processing software, modem performance depends on the processor's ability to execute a variety of software tasks in real time. Those tasks fall into two major groups: tasks that perform the transmitter function and the ones that perform the receiver function.

Most of these tasks involve complex computations such as adaptive equalization, demodulation, filtering ...Then implementing a complex algorithm on a real machine is not always efficient, since four operands have to be accessed with address computations and four multiplications have to be realized. The TS68930 digital signal processor gives the possibility of complex computations and permits to squeeze more performance into a single chip. In addition the associated chip to the DSP TS 7542 including programmable lowpass and bandpass filters, A/D and D/A converters, programmables clock generation and gain control (PGC) is useful in our application.

Our objective in the present work was to implement a multistandard modem giving the possibility of transmitting data at different speeds from 75 bps to 2400 bps. The corresponding CCITT and Bell recommendations are : V22, V22bis, V21, V23, Bell 103 and Bell 212A.

The V22bis is the most complex one, we will focus on it for it needs adaptive equalization, timing and carrier recovery.

The V22bis is a 2400 bps, full duplex, two-wire modem. In accordance with the recommendation of CCITT, it uses a separate carrier frequencies of 1200 Hz and 2400 Hz, and Quadrature Amplitude Modulation (QAM) technique.

For the non DSP tasks (displays, network-control, etc...), a host microprocessor is simply connected through the system bus section of the DSP to accommodate data exchange between the control processor and the DSP.

In paragraph 2 we review the DSP peculiarities. Key aspects of the V22bis transmitter and receiver are described in sections 3 and 4. The analysis of different functions is presented in simulation step in section 5. Finally in sections 6 and 7 we discuss implementation results on the DSP and the possibility for integration of additional low-rate modem standards in the same chip.

2. THE TS 68930 PROCESSOR

This DSP is a SGS-Thomson digital signal processor realized in a 2-µm NMOS process with 160 ns cycle time [1].

The highly parallel architecture of the DSP fits the inherent parallelism of the algorithms. The originality of the DSP is the availability of the complex arithmetic in its instruction set. The advantage of the complex architecture of the DSP over conventional real architectures is that for the same instruction cycle value, the DSP computes the complex multiplications two times faster. Complex multiplications are realized by using the inherent parallelism in the computation of four simultaneous real multiplications. This feature has been realized by adding pipeline registers and extra circuitry around the real parallel multiplier. The pipeline is hidden from the user at the instruction cycle level and it allows to double the rate of multiplications by decreasing the delay of the combinatorial logic. The complex arithmetic capability simplifies drastically the program development and offers high level programming facilities to the user.

In the programmable architecture of the DSP, real and imaginary parts of the operands are accessed sequentially in two basic cycles and the complex multiplication is achieved in two basic cycles. This results in a complex instruction cycle which is only twice than the one of the real mode, as opposed to the conventional real structures which is four times.

The internal architecture of the DSP is designed around three 16-bit data busses: L BUS and R BUS provide two operands from data memories or data registers to the arithmetic logic unit (ALU) or multiplier (MULT), while the third bus, Z BUS, saves the previous results from the ALU towards data memories or registers, all in one instruction cycle. The 32-bit instruction bus offers a high parallelism in the multibus structure and allows the realization of several operations in the same instruction cycle. Two 32-bit accumulators (A, B) and a pipeline FIFO (4x16-bit) memory are provided at ALU output. Two 128x16 bit internal RAM memories (XRAM, YRAM) can be accessed simultaneously by data busses. Data constants are stored in a separate 512x16 bit data ROM (CROM), and 4 K x 16 bit external ram (ERAM) can be accessed by the processor. An internal interface connected to the system bus allows the exchange of messages with another processor in a multiprocessor architecture without adding external logic. In our case the exchange of data with a host microprocessor is made through the MAILBOX procedure of the TS 68930 .

One important characteristic of this DSP is the possibility to set the computational mode in one of the following modes; real 16 bit, complex 2x16 bit, or 32 bit double precision .

The DSP family contains an additional chip for modem applications. It consists of a programmable clock, a 12-bit D/A converter with associated programmable attenuation analog lowpass filter, and a 12-bit A/D converter with programmable bandpass and programmable gain filters.

3. TRANSMITTER

Depending on the bit rate selected by the controller, the transmitter section (Fig.1) converts the incoming digital bit stream to an analog form compatible with the telephone channel. First, the data is scrambled in a pseudo-random fashion, making the spectrum of the transmitter output resemble white noise to use the channel bandwidth more efficiently. This operation eases the recovery of the carrier, the timing signal, and the channel equalization at the receiving end.

After "whitening" the output spectrum, the transmitter converts the scrambled serial bit stream into a parallel multibit word called symbols. For V22bis at 2400 bps, four bits define a symbol, and 16 symbols are used. The symbol rate is therefore one-fourth of the bit rate, or 600 symbols/s.

The encoder maps each symbol into a sequence of amplitudes and phases encoded symbols at a modulation rate of 600 bauds. Since the phase information is usually encoded differentially, each symbol generates a change from the previous phase rather than generating an absolute phase. The result is a complex number representing the desired amplitude and phase of the carrier for each symbol interval.

Complex output base band samples are then synthesized at a rate of 7200 samples per second with 2 bauds FIR filter which shapes the transmitted signal for a square root of raised cosine spectrum with 80% roll-off factor. The modulator performs a complex multiplication with 7200 samples/sec of the 1200 or 2400 Hz carrier, thereby forming a 7200 sampled/sec version of the real bandpass output signal. An IIR filter is then activated to provide compromise amplitude and time delay equalization for line transmission. The output level is scaled by prestored coefficients corresponding to settable transmit power levels. Output signal data is transferred in 12 bit words at

7200 samples/sec to an external digital to analog converter and smoothing lowpass filter. These 12-bit D/A converter and smoothing lowpass filter change the real output of that filter to analog form at a rate of 7200 samples/sec which becomes the modem's audio output.

4. RECEIVER

The key functions of the V22bis receiver program are shown in the block diagram of fig.2. The receiver section, which recovers the transmitted data, is not as straightforward as the transmitter. At the front end of the receiver a continuous lowpass filter (LPF) limits the bandwidth of the line signal in order to avoid the aliasing after the sampling operation.

Input signal data is received from 12 bit analog to digital converter at 7200 samples/sec The sample timing phase of the A/D is controlled by a counter whose modulus is programmable from the DSP timing recovery algorithm. Note that the 32 bit word-length of the DSP in double precision mode ensures that all required AGC and carrier detect functions can be implemented with adequate precision in firmware internal to the DSP.

The AGC controler is implemented within the processor without any external hardware. During the training sequence which is performed using the V22 constellation which contains only four points with constant amplitude, the AGC continuously calculates the energy of 12 subsequent samples of the input signal and tries to keep it on a fixed level. After a fast start-up period, when shifting to the V22bis modem, the AGC is programmed as to operate with a minimal ripple calculating the energy on large number of samples.

As in the transmitter, an IIR compromise equalizer is used in the receiver path for line amplitude and group delay equalization . The resulting bandpass signal is demodulated by multiplying the received signal by the samples of the local carrier. this demodulation is incoherent since the receiver carrier is not synchronized with the transmitter one. It will be completed later by the carrier recovery loop. Lowpass FIR matched filters are then employed to remove the double carrier component and to produce complex baseband samples at 7200 samples/sec.

The 600 Hz complex baseband signal resulting from demodulation and matched filtering is then supplied to T spaced complex transversal filter for channel equalization.

The modem receiver's adaptive equalizer accounts generally for the largest part of the total processing demand. It consists of a filter routine and a coefficient adaptation algorithm. The equalizer filter uses a finite-impulse-response structure, while the coefficient adaptation employs a least-mean-squares algorithm. A subroutine for the filtering portion of the equalizer demonstrates the processor's efficiency in dealing with complex numbers. Both the samples and the coefficients have real and imaginary parts. Coefficients and samples are stored in data memory (XRAM and YRAM), enabling them to be fetched simultaneously. Each time a new error vector becomes available, the coefficients get closer to their ideal values. A subroutine for the adaptation algorithm updates each complex coefficient in only 22 cycles.

An error computation compares the decision output to the equalizer output and calculates an error vector. As long as the decision is correct, the error vector indicates how far the received signal deviates from its ideal amplitude and phase.

The timing recovery block (fig.3) is constituted of three filters. The passband signal coming from the A/D converter is fed to two symmetric filters. The outputs of these filters are multiplied one the other and filtered through a narrowband filter centered on the baud frequency. The maximum of the signal is tracked during the training sequence. When the modem is running , the two samples amplitude around the maximum give the necessary information to control the A/D sampling phase.

A decision directed phase locked loop is used to correct for the carrier phase and frequency offset as well as the phase jitter impairments present in the received signal. Figure 4 shows the block diagram of the complete loop. The phase detector calculates the phase error based on the signals at the input and the output of the decision device. This phase error is fed into a second order loop, which consists of a proportional plus integral filter and a phase rotator. The phase rotator is a complex oscillator analogous to the VCO in a standard PLL.

The carrier recovery loop compensates for the phase error of the incoherently demodulated signal. Its operation is based on the decision feedback principle. The carrier recovery loop should also track the phase perturbations of the received signal, such as frequency offset , phase jitter and hits.

The receiver's last two blocks invert the operations performed by the first three blocs of the transmitter. The decoder maps the received amplitude and phase into a symbol and converts it to a multibit stream. Descrambling the stream recovers the original data.

5. SIMULATION

The first step before the final implementation on the DSP, was to perform an entire computer simulation very close to the behavior of the modem implementation in the DSP. This simulation is performed by an interactive software tacking into account the main perturbations which are encountered in the channel: a simulated 3002 FCC line, a phase jitter, a frequency shift and an additive white noise (Fig. 5). It allows an analysis of different functions. In particular the sensitivity of the equalizer, the timing recovery and the carrier

recovery loop to differents perturbations and to the control parameters variations.

In order to facilitate implementation of algorithms in fixed point arithmetics, and thus to make possible to verify and to validate results for implementation in the PSI language, the realization of a software tool (with the help of high level language) is necessary.

This step consists then to simulate, in FORTRAN language, algorithms of transmission and reception of the V22bis modem in fixed point arithmetics taking into account the DSP processor internal architecture. This approach facilitates comparison and verification of the results.

While input signal is from 12bit A/D converter, we assume that this signal is in ±1.0 interval. In our simulations, data in the analyzed window, are normalized with the absolute value of the maximum value. This normalization conditions the dynamic of variables directly related to the input signal. This simulation has been systematically used by a redefinition of elementary arithmetic operations. The truncature and the round off effects are taken into account within the new operands. On the other hand, the numerical results of the implementation in DSP language and those obtained by simulation with a fixed point arithmetics are identical.

6. IMPLEMENTATION

The implementation is organized in two major parts: monitor and tasks for transmitter and receiver algorithms. The monitor is a program controller allowing to organize tasks depending on the transmission mode and reception clocks phase

The transmitter and receiver software was implemented in the DSP assembly language. The total number of required instructions in program memory for transmitter receiver is much less than the available 1200X32bit ROM space of the DSP. This suggests that several other modem modes and other functions are implemented together with V22bis on a single DSP processor.

7. PERFORMANCE RESULTS

A full-duplex modem has been successfully implemented and tested using the DSP. Figure 6 shows the display of the received complex signal points prior to the decision block.

8. CONCLUSION

High performance V22bis voiceband data modem algorithm have been implemented for a single digital signal processor with its associated chip TS 7542 The approach of using a programmable processor resulted in a development effort to obtain working hardware with excellent performance. In addition other low rate transmission standards are implemented in the same chip without adding external hardware. The modem were tested under different channel conditions.

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Fig. 1 : The transmitter block diagram

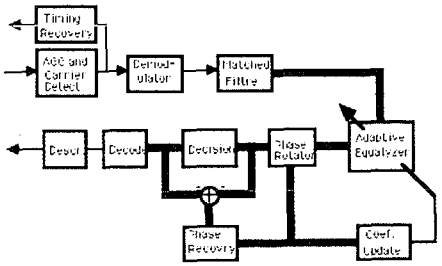

Fig. 2 : The receiver block diagram

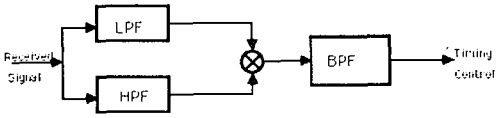

Fig. 3 : The timing recovery block diagram

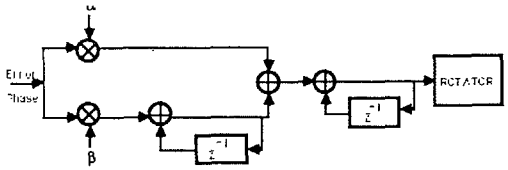

Fig. 4 : The carrier recovery block diagram

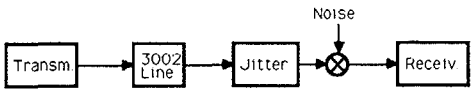

Fig. 5 : The simulation block diagram

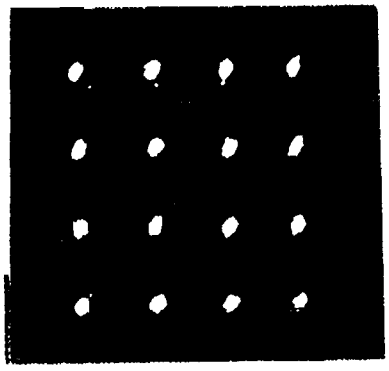

Fig.6 : The signal constellation